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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/633,362	DIJKSTRA, WILCO	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17-36 and 38-42* is/are rejected.

7)☒ Claim(s) *16 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 29 January 2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2163.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9-10 and 30-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear how the limitation "any other logical shift operation" changes the scope of the claims. The limitation does not state what is excluded by the term "other". Examiner suggests changing the limitation to "any logical shift other than any of said predetermined number of bits" or something similar. Examiner assumes for the purpose of examination that the limitation exclude a shift of one predetermined number of bits.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10, 14-15, 17-19, 21-31, 35-36 and 38-40 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Meier et al. (U.S. Patent No. 6,363,471 B1) herein referred to as Meier.

6. Regarding claim 1, Meier discloses a data processing apparatus comprising: a processor core (processor; see abstract, line 1) operable to process a sequence of instructions (see col. 4, lines 31-39), said processor core having a plurality of pipeline

stages (see fig 2; col. 8, lines 5-14), one of said plurality of pipeline stages being an address generation stage (AGU; see fig. 2) operable to generate an address associated with an instruction (Pseudo-address; see Fig. 3) for subsequent processing by said pipeline stages (address is output by the DTLB to Scheduler 36; see fig. 4), said instruction being one from a first group of instructions (Instructions using 16 bit addressing) or a second group of instructions (instructions using 32 bit addressing), said address generation stage comprising: address generation logic operable to receive operands associated with said instruction (Base, Index, SegBase, etc.; see Fig. 3), to generate a shifted operand (by shifter 68; see Fig. 3; col. 10, lines 15-20) from one of said operands, and to add together (by adder 64; see fig. 3, see col. 11, lines 1-3), in dependence on said instruction, selected of said operands and said shifted operand to generate said address for subsequent processing by said pipeline stages(The addition depends on whether the instruction is 16 or 32 bit; see col. 11, lines 10-14); and operand routing logic (logic in processor which routes data, which inherently exists) operable, in dependence on said instruction, to route operands associated with instructions from said first group of instructions to said address generation logic (Operands from either group will be eventually routed to the AGU; see fig. 3) and to route operands (such as mode or Displacement) associated with instructions from said second group (Either group will have these operands) of instructions via operand manipulation logic (see above) for manipulation of said operands (in any of the pipeline stages CAM 0, CAM 1, LP, IC, etc…; see fig. 2) prior to routing to said address generation logic (all these stages occur before the AGU stage).

Note that the claim does not limit the apparatus to only manipulate one group of instructions prior to sending them to the address generation unit. Additionally, there is no mention of how they are modified or for what reason. Something as simple as moving the operands from one part of the processor to another would fall under this claim language.

Regarding claim 2, Meier discloses the data processing apparatus of claim 1 (see above), wherein said instruction relates to a memory access and said address indicates a location in memory to be accessed (see col. 1, lines 60-65).

Note that inherently, by its definition, any computer address "relates to a memory access" and "indicates a location in memory to be accessed"

Regarding claim 3, Meier discloses the data processing apparatus of claim 1 (see above), wherein said first group of instructions comprises a first instruction which causes the processor core to logically add together two operands (all instructions in the first group will add together SegBase to Displacement; see Fig. 3), and a second instruction which causes the processor core to logically add together one operand (Base) to another operand (Index) logically shifted by one of a predetermined number of bits (all instructions in the first group will add together Index shifted by 1, 2 or 3 bits to Base; see Fig. 3; col. 10, lines 15-19).

Regarding claim 4, Meier discloses the data processing apparatus of claim 3, wherein said address generation logic is operable to generate said another operand logically shifted by one of a predetermined number of bits (by shifter 68; see fig. 3 and above regarding claim 3).

Regarding claim 5, Meier discloses the data processing apparatus of claim 3, wherein said second instruction causes the processor core to logically add together one operand to another operand logically shifted left by two bits (see Fig. 3; col. 10, lines 15-19).

Regarding claim 6, Meier discloses the data processing apparatus of claim 5, wherein said address generation logic is operable to generate said another operand logically shifted left by two bits (by shifter 68; see fig. 3 and above regarding claim 5).

Regarding claim 7, Meier discloses the data processing apparatus of claim 3, wherein said second instruction causes the processor core to logically add together one operand to another operand subject to only one preset (set at compile time) logical shift operation (all instructions in the first group will add together Index shifted by 1, 2 or 3 bits to Base; see Fig. 3; col. 10, lines 15-19).

Note that the shift value is preset because the shift is set when the instruction is written by a compiler and is set before execution and therefore preset).

Regarding claim 8, Meier discloses the data processing apparatus of claim 1, wherein said address generation logic is operable to perform only one predetermined logical shift operation (only the logical shift of the Index operand; see fig. 3; no other shifts are possible) and operands associated with all other logical shift operations required by instructions from said second group of instructions are routed via operand manipulation logic for manipulation of operands prior to routing to said address generation logic (all instructions are routed via operand manipulation logic prior to routing to said address generation logic; see above regarding claim 1).

Note that the limitation "is operable to perform only one predetermined logical shift" is extremely broad and the system of Meier can only perform one shift with the AGU (shifting the Index register). This shift is predetermined because the system can only perform the shift on that one operand and cannot shift any other operands.

Regarding claim 9, Applicant discloses the data processing apparatus of claim 3, wherein said second group of instructions comprises instructions which cause the processor core to logically add together one operand (Base) to another operand (Index) subject to any other logical shift operation (all instructions in the first group will add together Index shifted by 1, 2 or 3 bits to Base; see Fig. 3; col. 10, lines 15-19).

Note that any instruction that does not shift the index by 1 (or any other value) will still be in the second group.

7. Regarding claim 10, Applicant discloses the data processing apparatus of claim 9, wherein said operand manipulation logic is operable, in dependence on said instruction, to generate said another operand logically shifted by any other number of bits (by shifter 68; see fig. 3 and above regarding claim 9).

8. Regarding claim 14, Applicant discloses the data processing apparatus of claim 1, wherein said address generation logic comprises: operand generation logic operable to receive a first operand (Index; see fig. 3) associated with said instruction (see above regarding claim 1) and to generate a shifted operand representative of said first operand (by shifter 68; see fig. 3) shifted by a predetermined number of bits (all instructions in the first group will add together Index shifted by 1, 2 or 3 bits to Base; see Fig. 3; col. 10, lines 15-19

(Note that the number of bits is determined when the code is written and before it is executed and is therefore predetermined.);

operand selection logic (Included in shifter 68) operable, in dependence on said instruction, to select one of said first operand and said shifted operand (if Scale is 1, then the operand is not shifted and the operand is selected, otherwise, the shifted value is selected) as a selected operand; and addition logic operable to add a second operand associated with said instruction to said selected operand (by Adder 64; see fig. 3) to generate said address for subsequent processing by said pipelined stages (Psuedo-Address; see fig. 3; see above regarding claim 1).

9. Regarding claim 15, Applicant discloses the data processing apparatus of claim 14, wherein said first operand comprises `n`-bits, where `n` is a positive integer (32; see fig. 3), said operand generation logic receives said first operand over an `n`-bit input bus (a bus used to transfer 32 bits is a 32-bit bus) and provides said shifted operand on an `n`-bit output bus (see fig. 3;

Note that the value is shifted and output and sent to a 32-bit adder. The output bus must be 32 bits.),

said operand generation logic comprising: interconnection logic (Inherently there must be logic connecting the input and output) operable to couple lines of the `n`-bit input bus with lines of the `n`-bit output bus to perform the shift operation (by definition, this is how a shift works).

Regarding claim 17, Applicant discloses the data processing apparatus of claim 14, wherein said operand selection logic is operable to select one of said first operand and said shifted operand as a selected operand in response to a selection signal (Scale; see above regarding claim 14) generated by instruction decoder logic (whichever logic generates Scale which inherently exists).

10. Regarding claim 18, Applicant discloses the data processing apparatus of claim 14, wherein said addition logic is a two-operand adder (see col. 16, lines 21-35).

11. Regarding claim 19, Applicant discloses the data processing apparatus of claim 1, wherein said operand routing logic is operable to route operands in response to a routing signal generated by instruction decoder logic

(Note that there must be a signal to control the routing logic. Whatever creates this signal is considered to be part of the decoder logic.).

12. Regarding claim 21, Applicant discloses the data processing apparatus of claim 1, wherein said instruction is one of a load instruction (see page 3, line 16) and a store instruction.

13. Regarding claims 22-31, 35-36 and 38-40 and 42, these claims recite equivalent limitations as claims 1-10, 14-15, 17-19 and 21 are rejected under the same grounds.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 11-13, 20, 32-34 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy et al. (Computer Organization & Design The Hardware / Software Interface) in view of Meier.

Meier discloses all limitation of claims 11-13, 20, 32-34 and 41 with the exception of said second group of instructions comprises a subtractive instruction for which said address is generated by subtracting a subtrahend operand (Rc) from a minuend operand (Rb) associated with said instruction (instruction e; see page 3, lines 1-3), and said operand manipulation logic comprises subtraction operand generation logic operable to generate a negative representation of said subtrahend operand prior to routing to said address generation logic.

Hennessy teaches said second group of instructions comprises a subtractive instruction for which said address is generated by subtracting a subtrahend operand (b) from a minuend operand (a) associated with said instruction (Operation), and said operand manipulation logic comprises subtraction operand generation logic operable to generate a negative representation of said subtrahend operand (with the inverter; see Figure 4.16) prior to routing to said address generation logic (Adder, see Figure 4.16).

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Meier by adding logic to create an inverse of one operand prior to sending the operand to the address generation stage, as taught by Hennessy, in order to efficiently be able to handle subtraction of numbers without increasing the complexity of the address generation hardware.

Allowable Subject Matter

16. Claims 16 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not disclose or make obvious that said operand selection logic is a two-input multiplexer.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE R. MOLL whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 4/26/2008

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2163